Listing of Claims:

1. (Currently Amended) A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second semiconductor transistors and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor devices, and wherein the DC voltage characteristic data is obtained with the first and second semiconductor transistor devices operating in a subthreshold region; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices.

2. (Canceled)

3. (Currently Amended) The method of claim 1 ~~2~~, wherein the distribution of device mismatch comprises a distribution of Vt (threshold voltage) mismatch.

4. (Previously Presented) The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises retrieving said DC voltage characteristic data from a database.

5. (Currently Amended) The method of claim 1, ~~wherein the semiconductor devices comprise transistors and~~ wherein the step of obtaining DC voltage characteristic data for the device pair comprises measuring subthreshold DC voltage characteristic data in a subthreshold region of the transistors.

6. (Original) The method of claim 1, wherein the step of obtaining DC voltage characteristic data for the device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

7. (Previously Presented) The method of claim 1, further comprising the step of determining a variation in a device characteristic for a device of an integrated circuit comprising the device pair.

8. (Previously Presented) The method of claim 7, further comprising the step of assessing random variation of device mismatch of the semiconductor integrated circuit using variations in the device characteristic for each device of the integrated circuit as determined from distributions of variation of device mismatch for device pairs within the integrated circuit.

9. (Currently Amended) The method of claim 8, wherein the device characteristic comprises threshold voltage ~~and wherein the device pairs comprise transistors~~.

10. (Currently Amended) A method for characterizing device mismatch in a semiconductor integrated circuit, comprising the steps of:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit, wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region;

determining a distribution of Vt (threshold voltage) mismatch for the ~~a~~ selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit.

11. (Currently Amended) The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair of an integrated circuit comprises applying a constant gate voltage to a gate of the first transistor and varying V_{IN} applied to a gate of the second transistor such that ~~obtaining subthreshold DC voltage characteristic data while biasing~~ the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

12. (Original) The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair comprises separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

13. (Currently Amended) The method of claim 10, wherein the step of obtaining DC voltage characteristic data for a selected device pair comprises:

varying V_{IN} applied to gates of the first and second transistors such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

~~(i) serially connecting the a first transistor and the a second transistor;~~

~~(ii) applying a first gate voltage to a gate of the first transistor and a second gate voltage to a gate of the second transistor such that the first and second transistors are biased in a subthreshold voltage region, wherein at least one of the first and second gate voltages comprises a varying input voltage; and~~

~~(iii) determining output voltage of a node between the first and second transistors as a function of the varying input voltage.~~

14. (Canceled)

15. (Currently Amended) The method of claim 10 ~~13~~, wherein the step of determining a distribution of Vt mismatch for the selected device pair using the corresponding DC voltage characteristic data for the device pair, comprises the steps of:

determining a distribution of V_{IN} for a given output voltage, V_{OUT}; and

determining a distribution of Vt mismatch of the first and second transistors from the distribution of V_{IN}.

16. (Original) The method of claim 15, wherein the distribution of V_{IN} corresponds to a distribution of Vt mismatch between the first and second transistors when the first and second transistors each comprise an NFET.

17. (Original) The method of claim 15, wherein the distribution of V_{IN} corresponds to a distribution of one-half the Vt mismatch between the first and second transistors when the first and second transistors comprise an NFET and PFET.

18. (Original) The method of claim 10, wherein the integrated circuit comprises an SRAM (static random access memory) cell.

19. (Original) The method of claim 10, wherein the step of determining a Vt variation of transistors in the integrated circuit comprises determining a standard deviation of Vt variation of the transistors.

20. ~ 25. (Canceled)

26. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for a device pair comprising first and second semiconductor transistor devices, wherein the DC voltage characteristic data comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second semiconductor transistors and wherein V_{OUT} is obtained at a common node connection of the first and second semiconductor transistor devices, and wherein the DC voltage characteristic data is

obtained with the first and second semiconductor transistor devices operating in a subthreshold region; and

processing the DC voltage characteristic data to determine a distribution of device mismatch between the semiconductor devices.

27. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for characterizing device mismatch in a semiconductor integrated circuit, the method steps comprising:

obtaining DC voltage characteristic data for one or more selected device pairs of an integrated circuit, wherein the device pairs comprise pairs of neighboring first and second transistors in the integrated circuit, wherein the DC voltage characteristic data for a selected device pair comprises an output DC voltage V_{OUT} as a function of an input DC voltage V_{IN}, wherein V_{IN} is applied to a gate of at least one of the first and second transistors and wherein V_{OUT} is obtained at a common node connection of the first and second transistors, and wherein the DC voltage characteristic data is obtained with the first and second transistor devices operating in a subthreshold region;

determining a distribution of Vt (threshold voltage) mismatch for the ~~a~~ selected device pair using corresponding DC voltage characteristic data for the selected device pair;

determining a Vt variation of transistors in the integrated circuit using one or more determined distributions of Vt mismatch for selected device pairs; and

characterizing random variations of the integrated circuit using one or more determined Vt variations of transistors of the integrated circuit.

28. (Canceled)

29. (Currently Amended) The program storage device of claim 27 ~~28~~, wherein the distribution of device mismatch comprises a distribution of Vt (threshold voltage) mismatch.

30. (Canceled)

31. (Canceled)

32. (Previously Presented) The program storage device of claim 27, wherein the instructions for performing the step of obtaining DC voltage characteristic data for a selected device pair comprise instructions for separately measuring DC voltage characteristic data for each of a plurality of similar device pairs.

33. (Currently Amended) The program storage device of claim 27, wherein the instructions for obtaining DC voltage characteristic data for a selected device pair comprise instructions for performing the steps of:

varying V_{IN} applied to gates of the first and second transistors such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

~~(i) serially connecting the a first transistor and the a second transistor;~~

~~(ii) applying a first gate voltage to a gate of the first transistor and a second gate voltage to a gate of the second transistor such that the first and second transistors are biased in a subthreshold voltage region, wherein at least one of the first and second gate voltages comprises a varying input voltage; and~~

~~(iii) determining output voltage of a node between the first and second transistors as a function of the varying input voltage.~~

34. (New) The program storage device of claim 27, wherein the instructions for obtaining DC voltage characteristic data for a selected device pair of an integrated circuit comprise instructions for performing the steps of:

applying a constant gate voltage to a gate of the first transistor and varying V_{IN} applied to a gate of the second transistor such that the first and second transistors of the device pair are maintained in a subthreshold region of operation; and

determining V_{OUT} as a function of the varying V_{IN}.

35. (New) The program storage device of claim 27, wherein the instructions for determining a distribution of Vt mismatch for the selected device pair using the corresponding DC voltage characteristic data for the device pair, comprise instructions for performing the steps of:

determining a distribution of V_{IN} for a given output voltage, V_{OUT}; and

determining a distribution of Vt mismatch of the first and second transistors from the distribution of V_{IN}.

36. (New) The program storage device of claim 35, wherein the distribution of V_{IN} corresponds to a distribution of Vt mismatch between the first and second transistors when the first and second transistors each comprise an NFET.

37. (New) The program storage device of claim 35, wherein the distribution of V_{IN} corresponds to a distribution of one-half the Vt mismatch between the first and second transistors when the first and second transistors comprise an NFET and PFET.

38. (New) The program storage device of claim 27, wherein the instructions for determining a Vt variation of transistors in the integrated circuit comprise instructions for determining a standard deviation of Vt variation of the transistors.